REMARKS

Claims 1-8, 10-14, 16-25, 27-36, 38-43, 45, and 46 were pending in the above-identified application. Of these, claims 1-8, 10, and 11 are allowed; claims 12-14, 16-25, 27-30, 34-36, and 40-43, are rejected; and claims 31-33, 38, 39, 45 and 46 are objected to. Applicants, having amended the claims, respectfully request reconsideration.

Issues and Objections Relating to the Drawings

The examiner objects to the drawings for failing to support features of claim 3. With reference to Figure 7, for example, the examiner remarks that "the drawings must show (1) a comparator, (2) two sampled data streams, and (3) expected data" (Office Action, page 2). Applicants respectfully disagree: Figure 7 fully supports each of these claim elements.

First, as to the "comparator," the actual claim language is "comparison circuit." Figure 7 depicts an XOR gate that applicants refer to as "comparison circuit 755" (Para. 0050). The two "sampled data streams" find support at the outputs of samplers 705 and 710, which sample "input data on the same input terminal Din" (Para. 45) to produce respective sampled data streams. Lastly, the "expected data" finds support in the contents of shift register 730. In a margin-test mode described in connection with Figure 7, "the expected data is the input data sampled by sampler 705 and captured in shift register 730" (Para. 0049). Figure 7 thus includes the comparison circuit, two sampled data streams, and a source of expected data.

The examiner is also concerned that "the drawings must illustrate the comparator being operatively able to compare either one of the first and second data streams with the expected data via the comparator," and believes none of the drawings provides the requisite illustration (Office Action, page 2). Applicants once again disagree.

Claim 3 recites the circuit of claim 1 in which "the comparison circuit is adapted to compare at least one of the sampled-data streams with expected data." In the embodiment discussed in applicants' paragraph 0049,

> In the margin-test mode, each of multiplexers 715 and 720 selects its "one" input. The output of sampler 705 is thus conveyed to shift register 730 and the output of sampler 710 is conveyed to shift register 725....In this case, the expected data is the input data sampled by sampler 705 and captured in shift register 730. A voltage-control signal CV2 and timing control signal CT2 allow a tester or test personnel to alter the reference voltage and received

> clock RCK2 as necessary to probe the margin boundaries for sampler 710. Similar control signals CV1 and CT1 afford similar control over sampler 705 and are set to appropriate levels to ensure sampler 705 correctly captures the input data.

The outputs of registers 725 and 730 thus convey sampled data streams to comparison circuit 755. In the foregoing paragraph, multiplexers 715 and 720 allow comparison circuit 755 to compare e.g. the data from sampler 710 with the expected data in register 730.

Deriving the expected data an incoming data signal is advantageous because "it is not necessary to store expected data in advance or to provide a dedicated source of expected data" (Para. 0050). Other advantages are noted in paragraph 0050, but are omitted here for brevity. In any event, Figure 7 and the referenced text of applicants' specification support claim 3, so the objection to the figures as failing to support claim 3 should be withdrawn.

Rejections Under 35 USC §103

Claims 12, 13, 16-19, 21, 23, 24, 26, 27, 34, and 40-43 stand rejected as unpatentable over Matsumoto et al. in view of Lee et al. Applicants respectfully disagree.

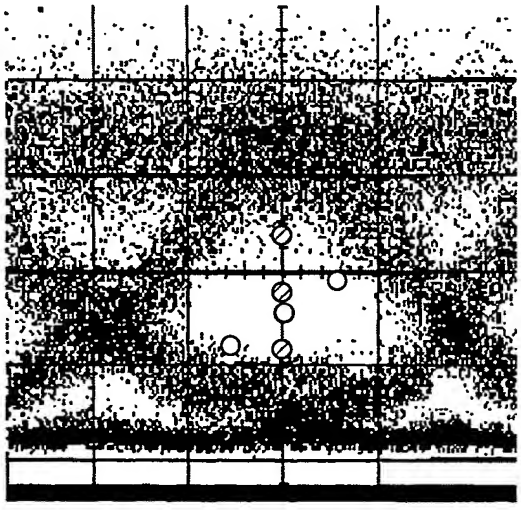
Claim 12 recites a method in which one series of input symbols is sampled using two clock signals of different phases to produce a first and a second series of sampled symbols. The two sets of sampled symbols are captured using different sample voltages. The examiner considers the method obvious over Matsumoto in view of Lee.

Applicants understand the examiner's argument to be as follows: Matsumoto discloses a method in which data is sampled at different voltages using a common clock signal, and Lee discloses a similar method in which data is sampled at different clock phases using a common reference voltage. It would be obvious to combine the sample voltages of Matsumoto with the different sample phases of Lee "because it would permit more flexibility in the reception and analysis of the input data by permitting the detection of data edges" (Office Action, page 5). As explained below, however, the proposed modification would render the system of Matsumoto unsatisfactory for its intended purpose. As such, the references cannot be said to provide the requisite suggestion or motivation for the modification the examiner is proposing (See MPEP 1243.01(V), citing *In re Gordon,* 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984)). The rejection of claim 12 is therefore improper and should be withdrawn.

The examiner's modification is based upon Matsumoto's Figure 2 (see Office Action, page 4). That figure depicts a clock and data recovery circuit (CDR) 100 with a "three-value

decision circuit 101 for identifying the upper decision point at nearby H level, the central decision point at nearby central level, and the lower decision point at nearby L level of the input data signal..." (Matsumoto, [0098]). This and related circuitry monitors the upper and lower voltage boundaries of a signal eye to place the "central decision point" at an "optimum position" within the eye. "[T]he central decision point voltage Vth is near the optimum position in FIG. 8..." (Id. at [0117]). The circuit of Matsumoto's Figure 2 thus probes the upper and lower voltage boundaries of a signal eye using relatively high and low sample voltages to position a central decision point voltage Vth in the center of the eye.

Matsumoto illustrates the concept of centering a sample point within a data eye using the simple, symmetrical illustrations of Figures 6-9. In practice, signal eyes can be much less clean and symmetrical. For instance, Matsumoto's Figure 25 "is a view showing an example of [an] optical waveform after transmission" (Matsumoto, [0082]; See also paragraph [[0005]). Matsumoto's Figure 25 is reproduced below and modified slightly to illustrate how changing the relative phases of the Matsumoto sample points, as the examiner suggests, renders Matsumoto unacceptable for its intended purpose: namely, the so-modified Matsumoto circuitry can no longer be counted on to place the central decision point voltage Vth in the center of an eye.



OPTICAL WAVEFORM AFTER
600Km TRANSMISSION
AVERAGE OPTICAL POWER
-24[dBm]

Figure 25 of Matsumoto

Applicants have added cross-hatched and white circles to identify six sample points, each of which represents a voltage (Y axis) and phase (X axis) pair. Matsumoto teaches taking three sample points at the same instant but using different voltages, as is illustrated using the cross-hatched sample points. The upper and lower points represent points at which errors appear: it is evident from Figure 25 that centering the third sample voltage between the other two, as Matsumoto teaches, places that sample point near what Matsumoto considers the optimum position.

Now consider the white sample points. These are taken at different sample instants, and so identify errors at different voltage levels. As a consequence, the white sample point centered vertically between the higher and lower points is not centered vertically within the eye. Given the asymmetry of this eye, the greater the phase shift, the less vertically centered the middle sample point becomes. Altering the relative phases of the Matsumoto sample points thus prevents Matsumoto from identifying the optimum sample voltage, and therefore renders Matsumoto unacceptable for its intended purpose. The modification suggested by the examiner thus cannot be considered obvious. The rejection of claim 12 is therefore improper and must be withdrawn.

Claims 13, 16-19, and 21 depend from claim 12, and consequently distinguish the examiner's combination of Matsumoto and Lee for the same reasons claim 12 distinguishes. The rejections of claims 13, 16-19, and 21 should therefore be withdrawn.

Claim 23 recites a method that is somewhat similar to the method of claim 12, and that was rejected for the same reasons claim 12 was rejected (see Office Action, page 7). The arguments presented above in connection with claim 12 apply equally to claim 23, so the rejection of claim 23 should be withdrawn. Claims 24, 26, and 27 depend from claim 23, so the rejections of those claims should also be withdrawn.

Claim 34 recites a communication system that includes a transmitter and a receiver. As amended, the receiver includes "a data filter" that finds support in receiver 1300 of applicants' Figure 13. "Data filter 1305 allows receiver 1300 to perform pattern-specific margin tests to better characterize receiver performance" (Ibid.). This filtering is beneficial, "as a receiver's margin may differ for different data patterns, due to ISI for example" (Ibid.). Absent some teaching of the data filter, the rejection of claim 34 should be withdrawn.

Claim 40 recites a receiver that includes "a data filter" with an input coupled to a data terminal and an "error-detection means." For example, data filter 1305 of applicants' Figure 13 is coupled to a data terminal Dout and XOR gate 1015, which serves as an error detector to produce an error signal Err. The examiner did not identify the recited data filter in either reference, so the rejection of claim 40 fails to establish a *prima facie* case of obviousness. The rejection of claim 40 should therefore be withdrawn.

Claims 41-43 depend from claim 40, and therefore distinguish the references for at least the same reasons. The rejections of claims 41-43 should therefore be withdrawn.

Claims 14, 25, 35, and 36 stand rejected as unpatentable over Matsumoto in view of Lee, as noted previously, and further in view of Best (U.S. Pub. No. 2002/0196883). The examiner cites Best for the proposition that "placing several circuit components on a single semiconductor substrate is notoriously known in the art" (Office Action, pp. 8 and 9).

Claim 14 depends from claim 12, and therefore distinguishes the references for at least the same reasons claim 12 distinguishes. Best does not make up for the deficiencies noted above in connection with claim 12, so the rejection of claim 14 should be withdrawn.

Claim 25 depends from claim 23, and therefore distinguishes the references for at least the same reasons claim 23 distinguishes. Best does not make up for the deficiencies noted above in connection with claim 23, so the rejection of claim 25 should be withdrawn.

Claims 35 and 36 depend from claim 34, and therefore distinguishes the references for at least the same reasons claim 34 distinguishes. Best does not make up for the deficiencies noted above in connection with claim 34, so the rejections of claims 35 and 36 should be withdrawn.

Claims 20, 22, and 28-30 stand rejected as unpatentable over Matsumoto in view of Lee, as noted previously, and further in view of Tobias (U.S. Pat. No. 7,188,261). Each of claims 20, 22, and 28-30 depend from claims noted above to distinguish the combination of Matsumoto and Lee relied upon for claims 20, 22, and 28-30. Tobias does not make up for the fact that combining Matsumoto and Lee in the manner suggested would render the system of Matsumoto unsatisfactory for its intended purpose. The rejection of claims 20, 22, and 28-30 should therefore be withdrawn.

Allowable Subject Matter

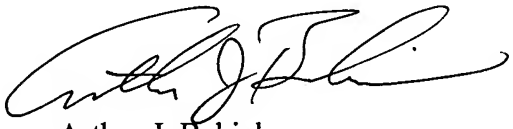
The examiner indicated that claims 1-8, 10, and 11 "contain allowable subject matter" (Office Action, page 11), and further that claims 31-33, 38, 39, 45, and 46 "would be allowable

if rewritten in independent form..." (Id. at page 12). Claims 31-33, 38, 39, 45, and 46 are all amended such that they are independent or depend upon an allowed base claim.

CONCLUSION

Applicants believe the claims to be in condition for allowance, and consequently request the examiner issue a notice of allowance. If the examiner's next action is other than the allowance of the pending claims, the examiner is requested to call applicants' representative at (925) 621-2113.

Respectfully submitted,



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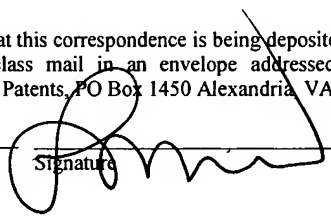
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